

High Speed Bi-Directional Digital I/O Board for PCI PIO-32DM(PCI)



* Specifications, color and design of the products are subject to change without notice.

Features

Since the board supports bus master, it is suited for fast-processing and controlling applications to control external devices with output of any digital pattern or to quickly sample digital input. The board is also equipped with synchronization control connectors to solve timing lag problems during channel expansion. However, since the board is susceptible to electrical disturbances, it should be used for applications with a short wiring distance and in quiet environment.

- With bus master, the board transfers data between the PC and board at a speed of 80MB/sec. (133 MB/sec. at maximum) without any burden on the CPU.
- "C-LogicDesigner" is available. You can download the application software "C-LogicDesigner" from Contec's website. You can handle the pattern generator as well as the logic analyzer feature without any programming.
- The board stores digital signals at a sampling rate of 20 MHz and can detect patterns (pattern input).
- The board can be used as a 20 MHz digital pattern generator (pattern output).
- A 1K-Word on-board FIFO memory is installed each for input and output.
- The 32-bit I/O lines can configure as either input or output, and 16-bit or 32-bit. The board can be set to 32-bit input lines, or 16-bit lines each for input and output, or 32-bit output lines.
- In addition to the digital I/O lines, control signals are available to start or stop pattern I/O. To achieve high-speed access to peripherals, the board also supports the REQ and ACK handshaking signals.
- The board is equipped with an SC connector to allow easy inter-board synchronization between the same or different boards.
- The board can be used not only for pattern I/O using bus mastering but also as a general-purpose digital I/O board. In general-purpose input mode, four input lines are available to interrupts (rising edge).
- Interrupts are set by the software, not by the hardware.
- The board is installed with a timer available to applications to accurately monitor time even when the board is used in Windows environment.

The PIO-32DM(PCI) is an interface board in compliance with the PCI bus specification and performs high-speed digital input and output application using bus mastering. This should be installed in a PCI bus slot.

The board can input and output a total of 32 TTL-level digital signals. Select input or output for each 16 signals.

Application Software "C-LogicDesigner" is supported. C-LogicDesigner has the pattern generator as well as logic analyzer feature. Windows Linux device driver is also available.

- * The contents in this document are subject to change without notice.
- * Visit the CONTEC website to check the latest details in the document.
- * The information in the data sheets is as of April, 2026.

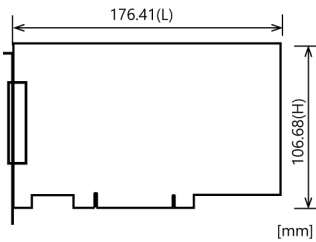
Specification

Specification

Item	Specification	
Digital section		
Number of I/O Channels	32-bit input lines, 16-bit input/output lines, 32-bit output lines (programmable)	
I/O signal level	TTL level (Equivalent to ALS245A)	
Data access method	General-purpose digital I/O or pattern I/O with bus mastering DMA	
Echo-back function	Available (at general-purpose output)	
Connector	Equivalent to PCR-96LMD (HONDA)	
Signal extension distance	1.5m (dependent on wiring environment)	
Pattern input	Sampling start trigger	Software start/External start/Pattern detection
	Sampling stop trigger	Software stop/External stop/End of transfer/Transfer error
	Sampling clock	Sampling timer/External clock input/handshake/SC connector
	Sampling timer	50ns - 107s 25ns unit
Pattern output	Generating start trigger	Software start/External start/SC connector
	Generating stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
	Generating clock	Output timer/External clock input/Handshake/SC connector
	Generating timer	50ns - 107s 25ns unit
Control signal	I/O signal level	TTL level (Input: equivalent to ALS541; Output: equivalent to LS125A)
	REQ signal (handshake)	Negative logic tL=50ns (Min)
	ACK signal (handshake)	Negative logic tL=50ns (Min)
	External start signal	Selection of rising/falling edge with the software
	External stop signal	Selection of rising/falling edge with the software
External clock input	f=10 MHz (Max)	
Bus master section		
DMA channels	2 channels (one each for input and output)	
Transfer bus width	32-/16-bit width	
Transfer data length	8 PCI Words length (Max)	
Transfer rate	80 MB/sec.	
FIFO	1K Word/ch.	
Scatter/Gather function	64 MB/ch.	
Synchronization section		
Control output signal	Selection of output signal with the software when specifying a sync master board.	
Control input signal	Selection of sync factor with the software when specifying sync slave boards.	
Max. board count for connection	16 boards including the master board	
Connector	PS-10PE-D4T1-B1 (IAE) or equivalent x 2	
Common section		
I/O addresses	Occupies 2 locations, any 32-ports and 64-ports boundary	
Interrupt	Errors and various factors, One interrupt request line as INTA	
Current consumption	5 VDC, 700 mA (Max)	
Operating conditions	0 - 50°C, 10 - 90%RH (No condensation)	
PCI bus specification	32bit, 33MHz, Universal key shapes supported *1*2	
External dimensions (mm)	176.41(L) x 106.68(H)	
Weight	130g	
Standard	VCCI Class A, CE Marking (EMC Directive Class A, RoHS Directive), UKCA	

- *1 This board requires power supply at +5V from an expansion slot (it does not work on a machine with a +3.3V power supply alone).
- *2 When the board No. is 7166, PCI bus specification is 32bit, 33MHz, 5V.

Board Dimensions



The standard outside dimension (L) is the distance from the end of the card to the outer surface of the slot cover.

Support Software

The name of the documents	Contents	How to get
Digital I/O Driver software API-DIO(WDM)	Driver software of digital input and output for Windows.	Download (ZIP)
Digital I/O Driver software API-DIO(LNX)	Driver software of digital input and output for Linux.	Download (tgz)
LabVIEW-support data acquisition library DAQfast for LabVIEW	This is a data collection library to use in the LabVIEW by National Instruments. With Polymorphic VI, our design enables a LabVIEW user to operate seamlessly. Our aim is that the customers to perform easily, promptly what they wish to do.	Download (ZIP)
Pattern Generator / Logic Analyzer for Windows C-LogicDesigner	C-LogicDesigner is software that uses a Contec high-speed bidirectional digital I/O device (32DM series) to generate digital signals and provide logic analyzer functions based on sampling. It is capable of automatically generating digital signal patterns and directly editing data in graphs, as well as generating signals based on a wide range of output conditions, checking signals that were sampled under specified conditions, saving data in files, searching data patterns, frequency calculation, and other functions.	Download (exe)

* Download the software from the CONTEC website.

Option

Item	Model	Description
Cable	PCB96PS-0.5P (0.5m)	Shielded cable with double-ended connector for 96-pin half-pitch connector
	PCB96PS-1.5P (1.5m)	
	PCB96P-1.5 (1.5m)	Flat cable with double-ended connector for 96-pin half-pitch connector
	PCA96PS-0.5P (0.5m) PCA96PS-1.5P (1.5m)	Shielded cable with single-ended connector for 96-pin half-pitch connector
Accessories	PCB96P-1.5 (1.5m)	Flat cable with single-ended connector for 96-pin half-pitch connector
	EPD-96A *1*2	Screw Terminal (M3 x 96)
	EPD-96 *1	Screw Terminal (M3.5 x 96)
	DTP-64A *1	Terminal Unit for Cables (M3 x 96P)

- *1 PCB96P or PCB96PS optional cable is required separately.
- *2 "Spring-up" type terminal is used to prevent terminal screws from falling off.
- * Check the CONTEC's Web site for more information on these options.

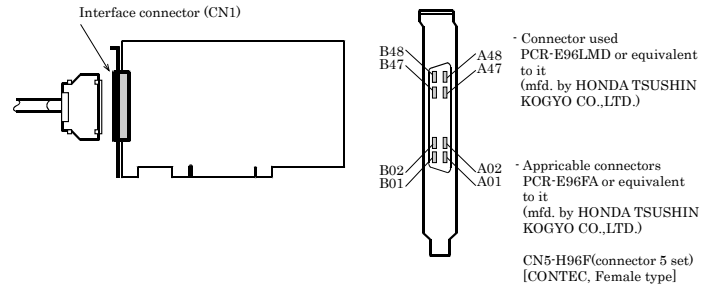
Packing List

- Board [PIO-32DM(PCI)]...1
- SC Cable (10cm) ...1
- Setup Guide ... 1
- Warranty Certificate ...1
- Serial Number Label...1

How to connect the connectors

Connector shape

To connect an external device to this board, plug the cable from the device into the interface connector (CN1) shown below.



	[49]	[1]			
Ground	GND	--B48	A48	---GND	Ground
Ground	GND	--B47	A47	---GND	Ground
Ground	GND	--B46	A46	---GND	Ground
External clock input	EXTCLK1	--B45	A45	---EXTCLK0	External clock input
Ground	GND	--B44	A44	---GND	Ground
External start signal	EXTSTART1	--B43	A43	---EXTSTART0	External start signal
Ground	GND	--B42	A42	---GND	Ground
External stop signal	EXTSTOP1	--B41	A41	---EXTSTOP0	External stop signal
Ground	GND	--B40	A40	---GND	Ground
REQ signal	EXTREQ1	--B39	A39	---EXTREQ0	REQ signal
Ground	GND	--B38	A38	---GND	Ground
ACK signal	EXTACK1	--B37	A37	---EXTACK0	ACK signal
Ground	GND	--B36	A36	---GND	Ground
Ground	GND	--B35	A35	---GND	Ground
Ground	GND	--B34	A34	---GND	Ground
I/O signal D07	DIOD07	--B33	A33	---DIOB07	I/O signal B07
Ground	GND	--B32	A32	---GND	Ground
I/O signal D06	DIOD06	--B31	A31	---DIOB06	I/O signal B06
Ground	GND	--B30	A30	---GND	Ground
I/O signal D05	DIOD05	--B29	A29	---DIOB05	I/O signal B05
Ground	GND	--B28	A28	---GND	Ground
I/O signal D04	DIOD04	--B27	A27	---DIOB04	I/O signal B04
Ground	GND	--B26	A26	---GND	Ground
I/O signal D03	DIOD03	--B25	A25	---DIOB03	I/O signal B03
Ground	GND	--B24	A24	---GND	Ground
I/O signal D02	DIOD02	--B23	A23	---DIOB02	I/O signal B02
Ground	GND	--B22	A22	---GND	Ground
I/O signal D01	DIOD01	--B21	A21	---DIOB01	I/O signal B01
Ground	GND	--B20	A20	---GND	Ground
I/O signal D00	DIOD00	--B19	A19	---DIOB00	I/O signal B00
Ground	GND	--B18	A18	---GND	Ground
I/O signal C07	DIOC07	--B17	A17	---DIOA07	I/O signal A07
Ground	GND	--B16	A16	---GND	Ground
I/O signal C06	DIOC06	--B15	A15	---DIOA06	I/O signal A06
Ground	GND	--B14	A14	---GND	Ground
I/O signal C05	DIOC05	--B13	A13	---DIOA05	I/O signal A05
Ground	GND	--B12	A12	---GND	Ground
I/O signal C04	DIOC04	--B11	A11	---DIOA04	I/O signal A04
Ground	GND	--B10	A10	---GND	Ground
I/O signal C03	DIOC03	--B09	A09	---DIOA03	I/O signal A03 / interrupt signal In03*
Ground	GND	--B08	A08	---GND	Ground
I/O signal C02	DIOC02	--B07	A07	---DIOA02	I/O signal A02 / interrupt signal In02*
Ground	GND	--B06	A06	---GND	Ground
I/O signal C01	DIOC01	--B05	A05	---DIOA01	I/O signal A01 / interrupt signal In01*
Ground	GND	--B04	A04	---GND	Ground
I/O signal C00	DIOC00	--B03	A03	---DIOA00	I/O signal A00 / interrupt signal In00*
Unconnection	N.C.	--B02	A02	---N.C.	Unconnection
Unconnection	N.C.	--B01	A01	---N.C.	Unconnection

- [] shows the pin No. of HONDA TSUSHIN KOGYO CO., LTD. specification.
* Can be used as an interrupt signal when used as general-purpose I/O.

Connection method to the external device -Data I/O-

Connecting the data I/O signal(DIOA0* - DIOD0*)

These lines input from and output to external devices and can be configured in 16-bit with the software.

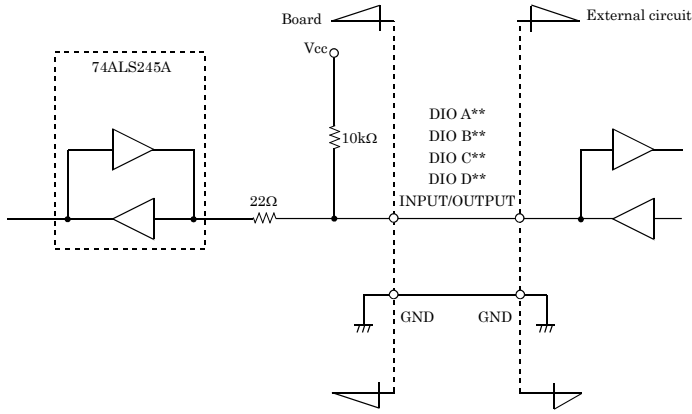
Input and output and setting procedures are the same whether these lines are used for general-purpose digital I/O or bus master transferring and they can be configured in three different settings as shown below:

I/O signal

Signal name	Setup1	Setup2	Setup3
DIOA00 - DIOA07	Digital input	Digital input	Digital output
DIOB00 - DIOB07	Digital input	Digital input	Digital output
DIOC00 - DIOC07	Digital input	Digital output	Digital output
DIOD00 - DIOD07	Digital input	Digital output	Digital output

When settings 1 and 2 are used for general-purpose digital I/O, DIOA00 through DIOA03 can be used as interrupts (rising edge).

Detailed Data I/O Signal Circuit



Connection method to the external device -Control I/O-

Connection to the control signal (EXT**)

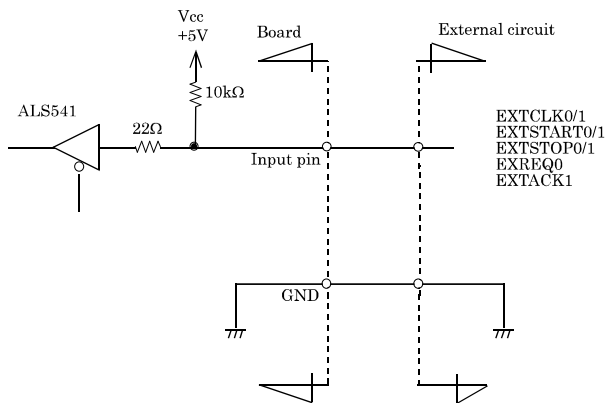
In order to control bus mastering from outside, five signals are provided each for pattern I/O. Before using the signals to be input as control signals please verify their pulse widths.

"0" at the end of a signal name indicates a pattern input signal and "1" a pattern output signal.

Signal name	Direction	Usage	Signal name	Direction	Usage
EXTCLK0	In	Pattern input clock	EXTCLK1	In	Pattern output clock
EXTSTART0	In	Pattern input start signal	EXTSTART1	In	Pattern output start signal
EXTSTOP0	In	Pattern input stop signal	EXTSTOP1	In	Pattern output stop signal
EXTREQ0	In	Pattern input REQ signal	EXTREQ1	Out	Pattern output REQ signal
EXTACK0	Out	Pattern input ACK signal	EXTACK1	In	Pattern output ACK signal

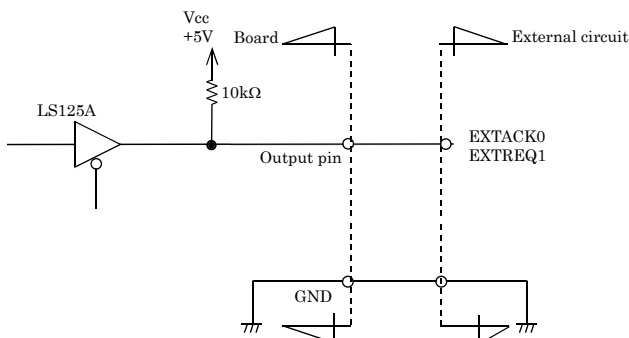
Detailed Control Input Signal Circuit

Control signals to be input include clock, start, stop, and handshake input signals.



Detailed Control Output Signal Circuit

Control signals to be output include handshake output signals.

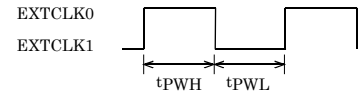


What is the Control Signal ?

External clock signal (EXTCLK0/EXTCLK1)

These signals input external pacer clocks. The maximum frequency is 10MHz.

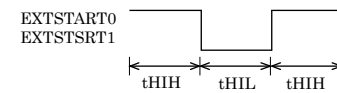
When the external clock input is set as the clock source, pattern input or output occurs at the falling edge of this signal.



tPWH : Clock pulse high width 50ns (Min.)
tPWL : Clock pulse low width 50ns (Min.)

External start signal (EXTSTART0/EXTSTART1)

These input signals start bus mastering with an external signal. The signal level is LVTTTL and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 50ns is needed at minimum.



tHIH : High level hold time 50ns (Min.)
tHIL : Low level hold time 50ns (Min.)

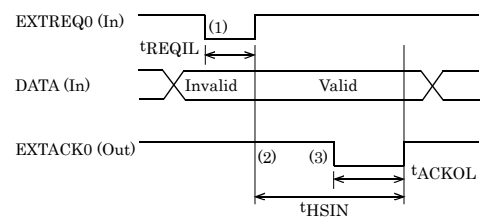
External stop signal (EXTSTOP0/EXTSTOP1)

These input signals start bus mastering with an external signal. The signal level is TTL and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 50ns is needed at minimum.

Handshake Signal (EXTREQ0/EXTACK0/ EXTREQ1/EXTACK1)

These signals handshake with external devices. The signal is TTL level and controlled with negative logic.

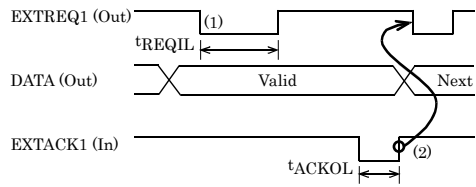
Input



tREQIL : EXTREQ0 low width 50ns (Min.)
tACKOL : EXTACK0 low width 100ns (Min.)
tHSIN : Handshaking time 100ns (Min.)

- (1) After setting the handshaking operation, the PIO-32DM(PCI) samples the EXTREQ0 signal and starts pattern input when it recognizes a low pulse of more than 50ns. Pattern data prior to that time is disabled.
- (2) The board generates a cycle to write data input from an external device to the PC memory by bus mastering.
- (3) At the end of writing data, the board outputs acknowledge signal EXTACK0 to notify the external device.

Output



t_{REQOL} : EXTREQ1 low width 100ns (Min.)
 t_{ACKOL} : EXTACK1 low width 50ns (Min.)

- (1) After setting the handshaking operation, the PIO-32DM(PCI) outputs the EXTREQ1 signal.
- (2) The board begins sampling acknowledge signals from external devices. The board recognizes the end with a low pulse of more than 100ns and, at the leading edge, starts preparing to output the next data.